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DIGITAL OHMMETER

by John Semyan

Goddard Space Flight Center

Greenbelt, Md.

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SUMMARY

This paper describes a unique method of digitizing resistive sensor outputs for telemetry. In the system proposed, the resistance to be measured comprises the unknown leg of a wheatstone bridge which is automatically nulled by sequentially adding the required binary values of resistance in series in the known leg. The states of the reed relay switches which control the binary balancing resistance then constitute a parallel digital word which represents unknown resistance. An absolute accuracy of ±0.05 percent is easily achieved.

A design example that was used to prove the practicality and accuracy of the system is presented in detail. Some consideration is given to possible improvements in power consumption, range of resistance measurement, and operating speed.

CONTENTS

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INTRODUCTION

An ohmmeter is a device that measures resistance in ohms. The *digital ohmmeter* described herein is one whose readout is inherently digital, rather than analog. Basically, the digital ohmmeter is a self-balancing bridge circuit. It may be compared to a standard servo system in that an error voltage is compared with a reference, after which corrective action is taken. Through a series of successive approximations, the bridge is brought close to balance.

The advantages of automatically nulling a bridge using the system described herein are numerous compared with an electromechanical system which uses servo motors, precision gear boxes, and precision potentiometers. The latter approach, common in high-accuracy ground systems for many years, has the following disadvantages:

1. Lubrication is required for many moving parts
2. Controlled environment is desired for efficient, long life operation
3. Precision required in manufacture and assembly of mechanical components is costly and time consuming
4. The final package is comparatively bulky and heavy
5. Power requirements are relatively high
6. An analog-to-digital converter is needed to supply data to digital telemetering systems
7. System redundancy is impractical

The digital ohmmeter virtually eliminates most of the above-mentioned disadvantages. The only moving parts in the proposed system are the reeds in hermetically sealed reed relays of proven reliability. Final packages may be small in size and weight, and consume little power. Direct digital readout is an inherent feature. Dynamic range is easily controlled, and accuracy of readout is readily predictable. Simple switching circuitry results in a long operating life.

The system design example shown in this paper demonstrates an absolute accuracy capability of better than 0.05 percent, the primary limitation being the number of bits provided for

readout. Higher orders of accuracy may be obtained by providing a greater number of bits and altering the bridge ratio.

The main limitation of the proposed system is its relatively low encoding speed. In the conservative system described, about 2 seconds is required to null the bridge and generate a single 8-bit resistance reading. Another limitation is the range of resistance which can be accommodated. Relay contact resistance can produce an error when very small resistances are switched, and maximum resistance is limited by stray capacitance effects. These limits depend on desired readout accuracy and dynamic range.

DESCRIPTION OF SYSTEM OPERATION

As stated previously, the method employed here in measuring an unknown resistance is to digitally null a bridge automatically. This is done by the successive approximations method, employing a binary adjustable resistance in the known leg of the bridge. Each resistor comprising this step-adjustable resistance is sequentially sampled and controlled, from the largest to the smallest binary value. When all have been sampled, the bridge is in a balanced condition within an easily defined percentage of error.

Reed relays are used as switches across each resistor in the known leg of the bridge. Before the sequential sampling process begins, a reset circuit *opens* all switches so that the binary adjustable resistor assumes a maximum value. This condition produces an error signal out of the bridge to an amplifier, and thence to a phase detector. Serial pulses, derived from a clock signal, are used to sequentially close the switches across the binary resistors. During the time that each binary resistor is being tried, the error signal out of the bridge is amplified and compared in phase with the bridge-drive reference signal. The output of the phase detector is then applied to circuitry that controls the condition of the respective switch. After the last–and smallest–binary resistor is sampled, the status of the switches constitutes a parallel digital word which represents the value of unknown resistance.

DESIGN EXAMPLE

Preliminary Considerations

The following design example illustrates the practicality of the concept. Before detailed design can proceed, a group of somewhat arbitrary design goals must be specified:

Unknown resistance range	900 to 1000 ohms
Allowable power dissipation in unknown resistance	1 milliwatt max.
Number of bits per data word	8
Encoding speed	approx. 2 sec (4 cps clock)
Available supply voltages	±6 volts d.c.

An 8-bit binary word provides 2^8-1, or 255, discrete coding levels, corresponding to about 0.4 percent of range uncertainty. The 10 percent measurement range of unknown resistance therefore should permit an absolute measuring accuracy approaching ±0.02 percent.

The long encoding time was chosen for system demonstration, since the logic operation is easily followed and visual readout is possible while the coder is cycling continuously. A 400 cps drive for the bridge was selected. This frequency must be considerably higher than the clock rate to allow effective carrier filtering at the phase detector output, but not so high that stray capacitance will be troublesome. A square waveform was chosen to permit use of a simple logical AND gate as a phase detector.

The maximum permissible power dissipation in the unknown resistance is specified because of self-heating effects which would have to be considered in a typical sensor application. A platinum wire temperature sensor, for instance, should have negligible self-heating to minimize error. Since 1 milliwatt has been specified as the maximum permissible power dissipating in the 1000 ohm sensor, the square wave driving voltage appearing across the sensor must not exceed the amplitude shown in the following calculation:

$$P = \frac{E_s^2}{R_s} ,$$

where

P = power dissipation,
E_s = sensor voltage (rms),
R_s = sensor resistance;

or

$$E_s = \sqrt{P R_s} .$$

For 1 milliwatt power dissipation and 1 kilohm resistor resistance,

$$E_s = \sqrt{(10^{-3})(10^3)} = 1 \text{ volt rms.}$$

Figure 1 shows a block diagram of the complete system.

Bridge Drive Circuits

The free-running bridge drive multivibrator used in the breadboard model (Figure 2) operates between ±6 volts dc at a frequency of approximately 400 cps. The output waveform is symmetrical to within 5 percent.

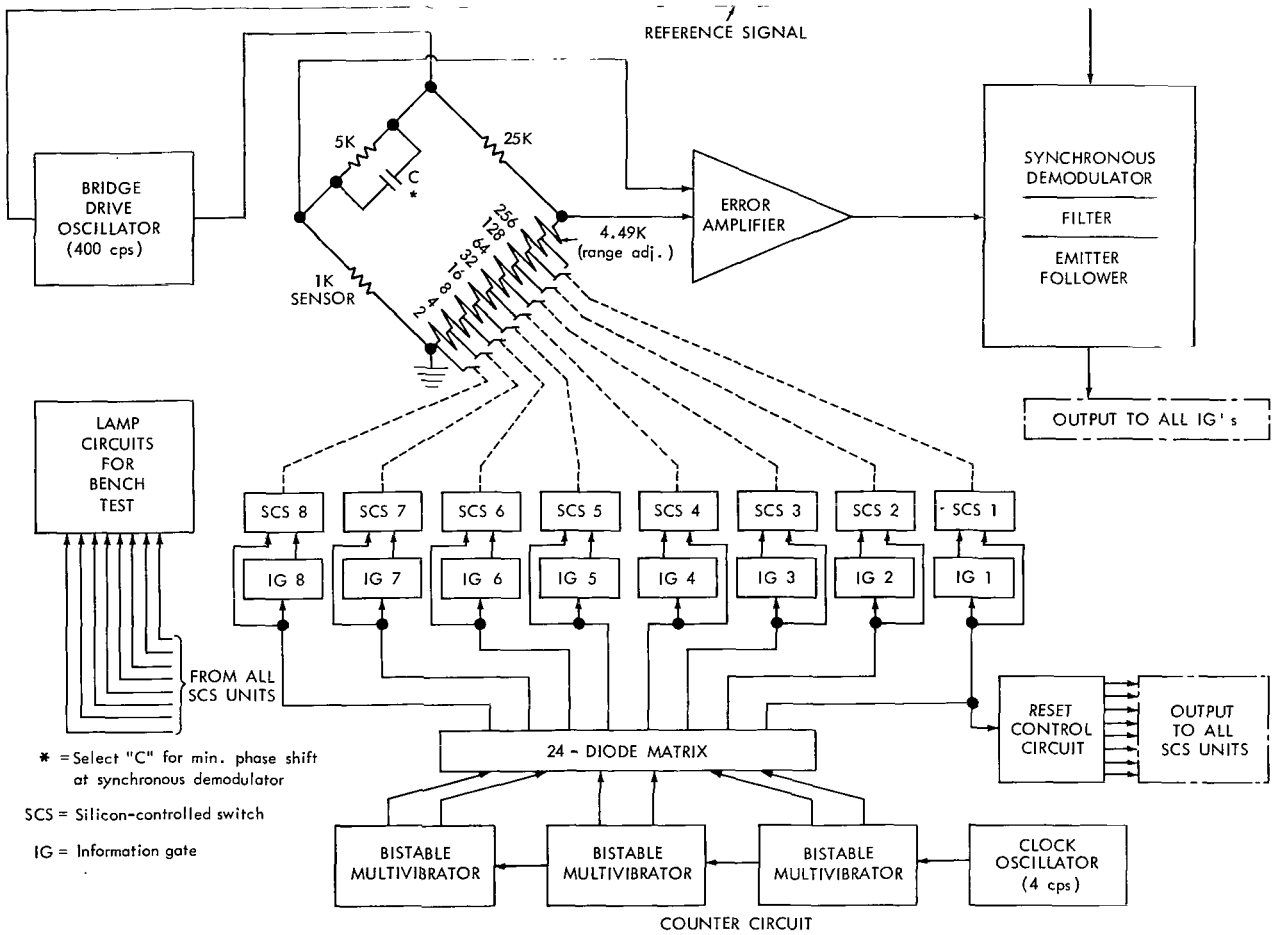


Figure 1–The digital ohmmeter.

Perhaps the most obvious bridge drive configuration uses a balanced transformer drive [Figure 3 (a)] and produces a single-ended output. The transformer is undesirable in this application because of the low-frequency square wave involved and because of the effects of interwinding capacitance. If the output and drive are interchanged, the configuration of Figure 3 (b) results. The drive is now single-ended with respect to ground, and the balanced output may be handled conveniently by a differential amplifier. The latter connection is considered preferable. The schematic diagram in Figure 2 shows the complete drive circuit.

Bridge Design

A 1:5 bridge ratio permits larger increments of resistance in the binary adjustable resistor, avoiding errors due to end-of-life reed relay contact resistance. Since 2 ohms is the smallest increment in the binary adjustable leg of the bridge, a change of 0.4 ohm in the sensor can be balanced out. An error of 0.4 ohm would constitute a 0.04 percent error in absolute sensor resistance. The unknown resistance specified has a range of variation from 900 to 1000 ohms. Therefore, the dynamic range of measurement is 100 ohms, or 10 percent, and an overall change of 500 ohms in the X5 leg of the bridge is necessary for bridge balance.

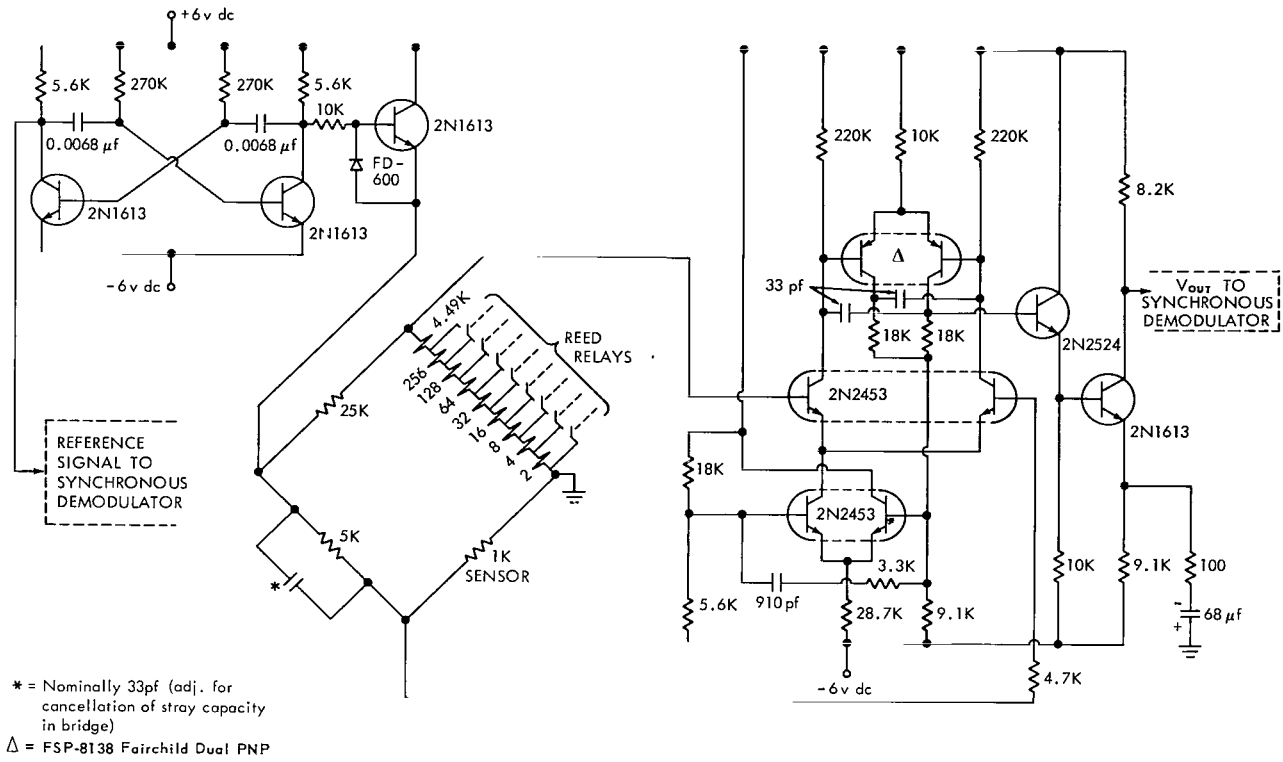
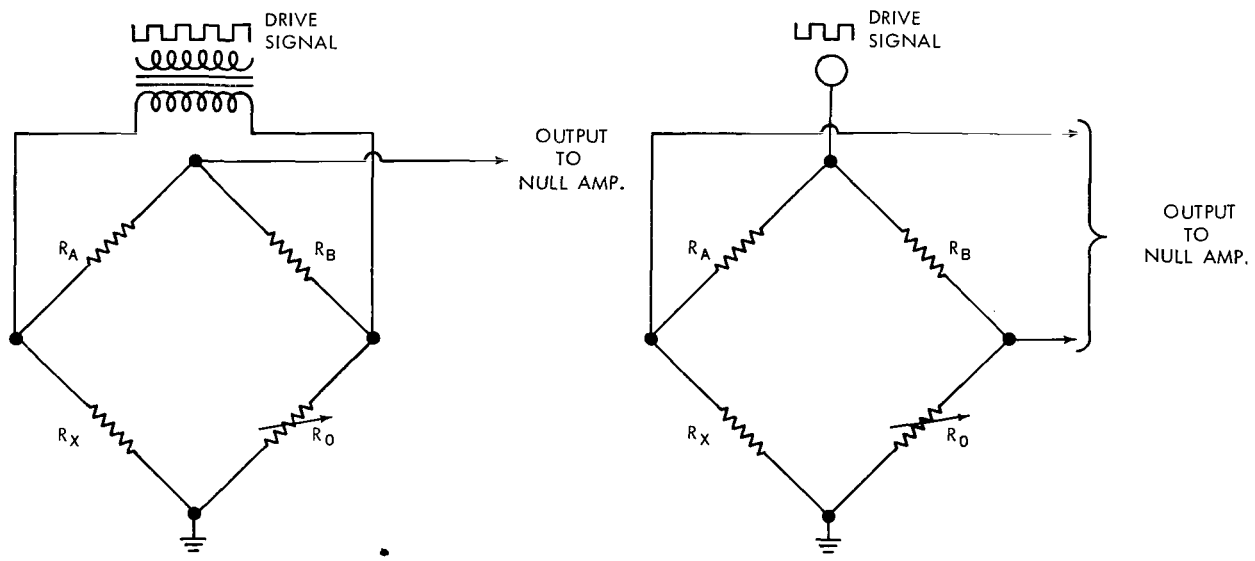


Figure 2—Bridge drive oscillator, bridge, and differential error amplifier.

Binary Values of Resistance (N=8 bits)	Binary Resistor Value (ohms)	Equivalent R in Sensor (ohms)
2^0	2	0.4
2^1	4	0.8
2^2	8	1.6
2^3	16	3.2
2^4	32	6.4
2^5	64	12.8
2^6	128	25.6
2^7	256	51.2

A 510 ohm range in the known leg of the bridge is achieved with binary resistor values as shown in the table, giving an actual measurement range of 898 to 1000 ohms.

The measured drive signal to the bridge is approximately 7 volts peak-to-peak, producing an average power dissipation of less than 1 milliwatt in the sensor for the 5:1 drive ratio selected. The differential



(a) Bridge connected for balanced drive and single-ended output

(b) Bridge connected for single-ended drive and balanced output

Figure 3—Two bridge drive configurations.

signal out of the bridge produced by a 0.4 ohm change in the sensor resistance, or a 2 ohm change in the X5 leg, may be calculated approximately as follows:

$$V_{out} = V_{in} \frac{\Delta R_0}{R_0 + R_B} = 7 \frac{2}{(5 \times 10^3) + (25 \times 10^3)} = 0.47 \text{ Mv P - P},$$

where

V_{in} = 7 v P - P (bridge driving voltage),
R_0 = 5×10^3 ohms (known leg of bridge),
R_B = 25×10^3 ohms [see Figure 3 (b)].

Thus, the error signal out of the bridge could range from 0 to a maximum of 0.47 Mv peak-to-peak when the 2^0 binary resistor is sampled.

Error Amplifier

The nominal gain in the error amplifier should be about ten times greater than that required to operate the phase detector from a 0.47 Mv input, to insure the validity of the least significant bit. This allowance also provides a margin for safe operation with fairly large, environmentally induced gain variations.

The minimum voltage gain required in the error amplifier may be computed as follows, allowing a factor of 10 excess of gain over that required to just operate the least significant digit:

$$A = \frac{KV_o}{V_{in}} = \frac{10 \times 1.2}{0.47 \times 10^{-3}} = 26,000 ,$$

where

V_o = 1.2 v, the peak-to-peak voltage necessary to saturate the AND-gate switch in the synchronous demodulator circuit;

V_{in} = 0.47 Mv as calculated for the smallest incremental bridge output;

K = 10, a nominal gain margin as explained above;

A = minimum gain required.

A high common-mode rejection (CMR) ratio in the error amplifier is necessary because the common-mode signal output would have the same effect on the synchronous demodulator as a differential error signal from the bridge. To insure a negligible error contribution, the equivalent common-mode input signal should be a factor of 10 below the differential input signal equivalent to a 1-digit error. Thus, for an amplifier gain of 26,000, the CMR ratio required would be

$$\frac{1.2 \times 26,000 \times 10}{1.2} ,$$

or about 108 db. Measured CMR ratio and gain for the amplifier shown in Figure 2 are 102 db and 30,000 respectively. These are considered entirely adequate for system test purposes.

Since a square wave signal is being amplified, the effect of phase shift—within limits—can be negligible. If operating frequency were to be changed greatly, then the frequency characteristics of the amplifier would require alteration. Frequency response of the amplifier design, as shown in Figure 2, is about 20 cps to 6.5 kc.

Synchronous Demodulator

The output of the error amplifier is capacitor-coupled to the lower transistor in the synchronous demodulator. The reference signal from the astable multivibrator is capacitor-coupled to the upper transistor. Refer to Figure 4. When both signals are *in phase* with each other, a negative output appears at the collector of the upper transistor. If the reference and error signals are *out of phase,* no negative voltage is produced at the output of the demodulator. A voltage divider adjusts the dc voltage level at the collector of the upper transistor to approximately +1.8 volts dc when no output signal is present. When error and reference signals are in phase, the

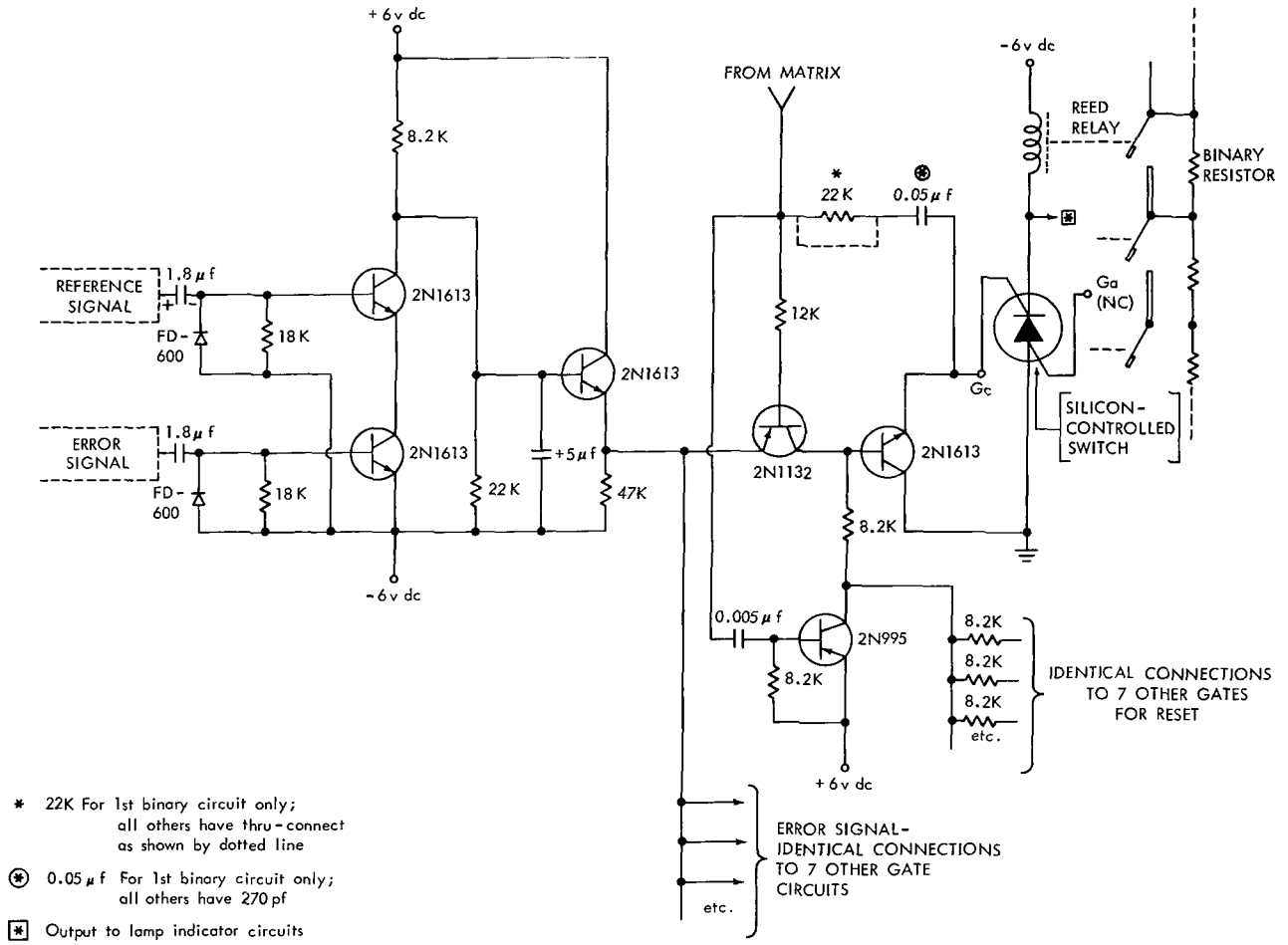


Figure 4—Synchronous demodulator, information gate, and silicon-controlled switch.

filter circuit produces a negative dc output voltage that maximizes at approximately -5 volts dc. The output of the synchronous demodulator is fed through an emitter follower to the eight gate inputs.

Clock Oscillator and Serial Pulse Generator

In the present system, an astable multivibrator or clock oscillator having an operating frequency of approximately 4 cps drives a counter as shown in Figure 5. The counter consists of three cascaded bistable multivibrators, which count down to a final output frequency of approximately 0.5 cps. The counter outputs connect to a twenty-four diode AND matrix. The diode cathodes are connected in a binary configuration to eight 51 kilohm resistors. At this point of connection the matrix supplies eight serial outputs that are used as sequential gate trigger signals. The 51 kilohm resistors are connected to a -6 volt source. Because of the loading effects of the gate, the swing of the matrix output pulses is approximately +2 volts to - 0.2 volt. Figure 6 shows a timing diagram of the system.

Control Circuits

The matrix outputs are connected to the bases of the eight gate transistors; also, they are fed through a differentiating network to the cathode gates of the silicon-controlled switches. The matrix output to the largest binary digit control circuit also is fed through a differentiating network to a reset circuit that is common to all eight binary digit control circuits. The reset pulse places all the silicon-controlled switches in an *off* condition; hence all binary resistors are series-connected in the bridge circuit (see Figure 4).

The same pulse that the reset circuit receives from the matrix is applied to another differentiating circuit, with a longer time constant than that employed to gate the reset circuit *on*. This negative-going pulse switches the silicon-controlled switch to an *on* condition so that the reed relay switch is closed, and the largest binary resistor is shorted out of the bridge circuit. This sampling of the largest binary resistor produces an error signal out of the bridge circuit that has a phase relation with the reference signal. If a positive signal is applied to the emitter of the gate transistor, the negative matrix output pulse turns the gate transistor *on* and applies the positive error signal to the base of a switching transistor which virtually shorts the cathode gate of the silicon-controlled switch to ground. Thus, the silicon-controlled switch is opened

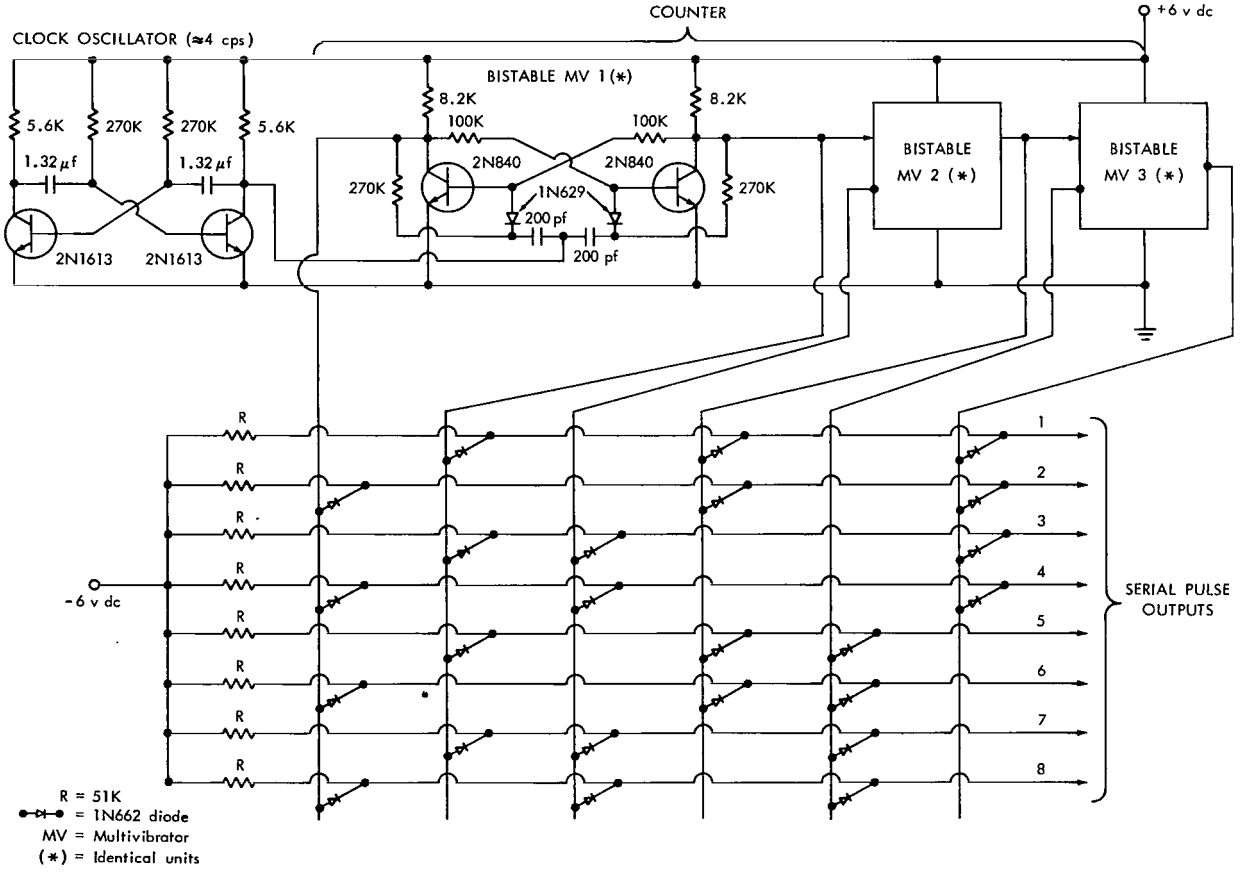


Figure 5—Clock, counter, and matrix circuits.

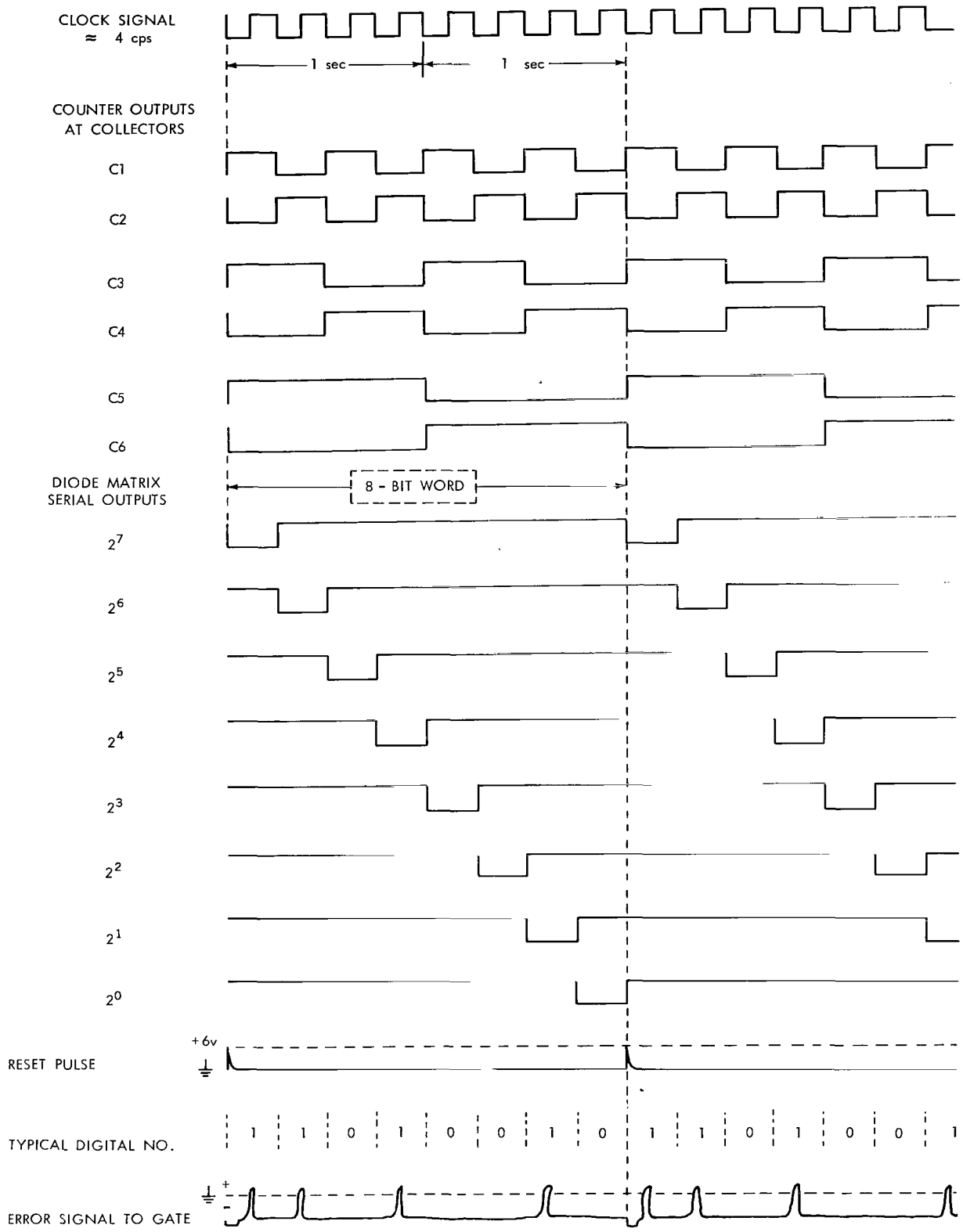


Figure 6–Timing diagram for digital ohmmeter.

and the largest binary resistor is again functional in the bridge circuit. If the error signal is negative, the gate never reopens and the largest binary resistor remains shorted out of the bridge. This process is then repeated for the remaining 7 binary digits.

The reset circuit is actuated only at the start of the sampling pulse for the largest binary resistor. The other control circuit operations take place during the sampling period for each binary resistor.

EXPERIMENTAL EVALUATION

The unit described herein performed as expected. A decade resistance box with 0.1 ohm increments of resistance was used as the unknown. A lamp indicator system, shown in Appendix A, was used as an output display. A plot of binary numbers versus resistance proved system performance and accuracy. Absolute accuracy was better than ±0.1 percent, the tolerance of the bridge resistors used.

The 4 cps clock frequency used in the example was experimentally increased to about 20 cps, without appreciable change to other parts of the system. Increasing bridge drive frequency should allow further increase in coding speed.

A ring counter circuit employing modular bistable elements was tried in place of the counter and diode matrix circuits. It operated very efficiently and would be preferred in a reliable flight package. A ninth serial pulse is easily provided for more reliable "reset" action and for a "transfer" pulse to a telemetry system or word buffer.

It is expected that a shunt-type gating system for the error signal circuit would permit a greater range of parameter variation and possibly simplify the control circuit. Also, the silicon-controlled switch might be replaced by a more easily controlled level-sensitive bistable circuit.

CONCLUDING REMARKS

No great amount of circuit refinement effort has gone into the development of this system. The design example presented here proves feasibility only. It readily can be seen that the demonstrated method is valid and that it may be adapted to many systems concerned with resistance measurement. The direct digital output makes the unit quite compatible with modern digital telemetry systems. It may be concluded that proper application of the basic scheme can result in a system of outstanding accuracy, coupled with high efficiency and inherent reliability.

ACKNOWLEDGMENTS

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Appendix A

Lamp Indicator System for Bench Check of Digital Ohmmeter

To facilitate bench checkout and demonstration of the system, miniature lamps were used to indicate the state of each bit. These are driven from the reed relay coils through separate amplifiers as shown in Figure A-1. A lighted lamp indicates a binary "1" and an *off* lamp, a "0". Actual unknown resistance is easily calculated as shown for the sample readout.

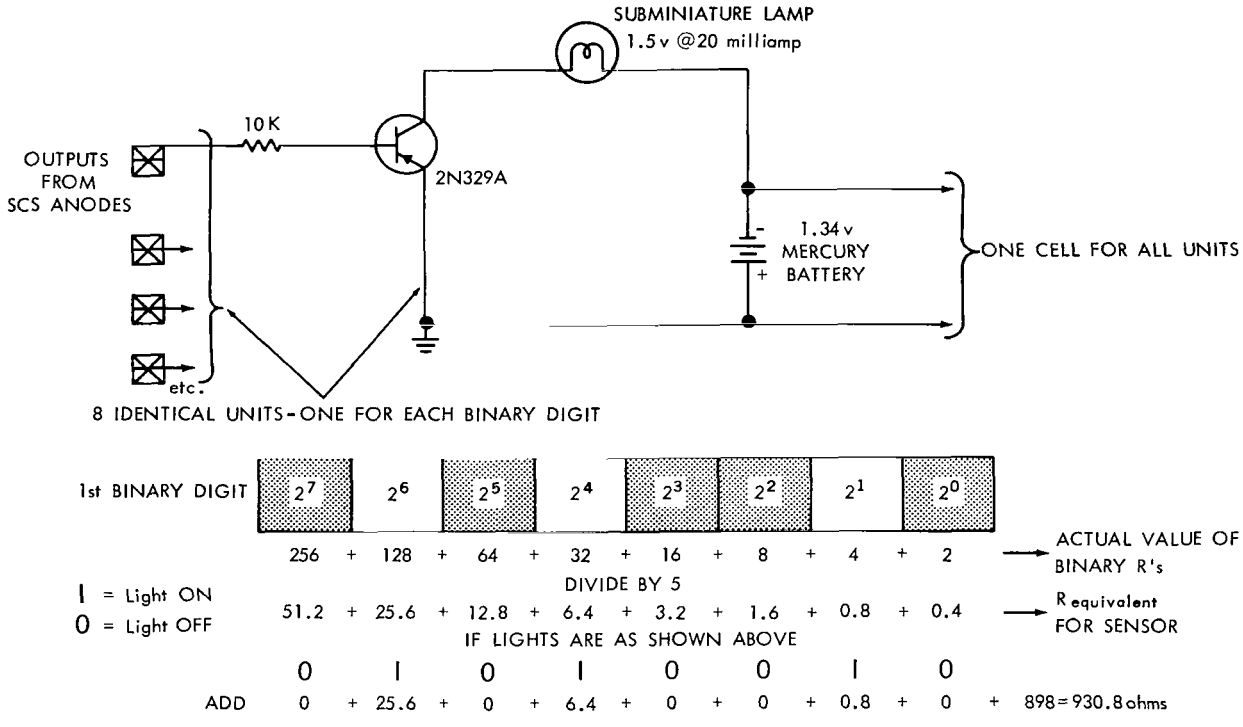

Figure A-1—Lamp indicator circuit for bench checkout of system.

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